

EPC9192 Audio Performance Recommendations

Document version: 1.1

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Status: preliminary engineering recommendations, pending confirmation of the revised EPC9558L schematic from the contributor.

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1. Review Scope

The revised EPC9558L schematic from the contributor is not currently present in this directory and remains pending confirmation. Until the confirmed file is supplied, no proposed schematic changes can be reviewed. There is also no improved BOM, PCB source, Gerber package, assembly drawing, or before/after measurement data in this directory. The recommendations below apply to the official EPC9192KIT and are not claims about changes already implemented.

Before modifying hardware, resolve these documentation and assembly questions:

1. EPC9558L C3 is 100 pF in the BOM, while the schematic note says 82 pF is mounted in CH1. Record the actual value on both modulator boards.
2. The EPC9192 BOM marks the Allegro ACS71240 current sensor position as empty and the MPS MCS1823 position as populated, while the guide describes the Allegro part as the default. Confirm whether each channel has a nominal 40 A or 45 A OCP threshold.
3. Confirm the actual L2 part. The documentation variously describes it as 14 A, 40 A peak, or greater than 40 A saturation current.
4. Record the population of EPC9558P D1-D4, R86, L1, L2, and all parts marked **EMPTY** in the BOM.
5. Record all PCB, schematic, BOM, and assembled-board revision labels. The supplied documents mix Rev. 1.0, Rev. 2.0, and Rev. 2.1 identifiers.

2. Official Baseline

The official design is already highly optimized in several areas:

- Two asynchronous, self-oscillating PFFB channels at approximately 600 kHz idle frequency.
- Approximately 40 dB loop gain at 20 kHz.
- EPC2307 200 V GaN FETs and an NCP51820 gate driver.
- Nominal 50 ns dead time set by EPC9558P R86 = 49.9 kohm.
- 10 uH output inductor and 0.68 uF polypropylene film capacitor.
- Ideal LC resonance of approximately 61.0 kHz.
- C0G/NP0 capacitors in critical EPC9558L timing and feedback positions.
- 0.1% thin-film resistors in important feedback positions.
- Published performance of approximately 0.005% THD at 1 kHz/10 W/4 ohm, 40 uV(A) output noise, and 121 dB SNR at the lower gain setting.
- Four-layer, 2 oz power-stage PCB, VIPPO thermal vias, top cooling, and local high-frequency bus capacitors.

This means that arbitrary op-amp, capacitor, cable, or semiconductor substitutions are unlikely to be useful. Every accepted change should produce a repeatable measured improvement without a stability, EMI, protection, efficiency, or thermal regression.

3. Recommended Order of Work

Priority	Experiment	Expected opportunity	Risk
P0	Audit actual component population and establish a baseline	Prevents testing the wrong configuration	Low
P1	Improve external power delivery and grounding	Lower rail modulation, hum, and channel coupling	Low to medium
P2	Test active Schottky diodes and dead time together	Lower high-current switching distortion and loss	High
P3	Tune turn-on and turn-off gate impedance	Lower ringing, timing error, and EMI	High
P4	Verify local bus and driver decoupling	Lower rail bounce and pulse-width modulation	Medium
P5	Characterize L1, L2, and C18 under current	Lower magnetic/filter distortion	Medium to high
P6	Improve PFFB sensing and grounding in a PCB revision	Lower feedback contamination and output impedance	High
P7	Improve analog and housekeeping rails	Lower idle noise and converter spurs	Medium
P8	Characterize two-channel beat products and crosstalk	Lower idle tones and inter-channel IMD	Medium to high

4. Baseline Measurement Plan

Do not judge modifications by listening alone. Record the following stock-board baseline before changing components.

4.1 Fixed Test Conditions

- Use balanced XLR inputs and open the +10 dB/J2 gain jumper unless the higher gain is specifically required.
- Use Kelvin voltage sensing directly at the output terminals, as required by the EPC guide.
- Use short, twisted supply and speaker conductor pairs.
- Record the exact high-voltage PSU, 12 V PSU, external capacitance, rail voltage, load, input level, airflow, heatsink, and ambient temperature.
- Warm the amplifier to a repeatable temperature before each test.
- Change one variable at a time and retain one unmodified channel or board as a control whenever possible.

4.2 Loads and Operating Points

Measure with 2, 4, and 8 ohm non-inductive loads at:

- Idle/no signal.
- 1 W, 10 W, 100 W, and the thermally permitted high-power point.
- 20 Hz, 100 Hz, 1 kHz, 6.67 kHz, and 20 kHz.
- Single-channel and simultaneous two-channel operation.
- Single-ended and BTL modes where applicable.

Then repeat stability and frequency-response tests with a documented simulated-loudspeaker network and representative speaker cables. The official limit for a purely capacitive load is 0.2 μ F; do not exceed it.

4.3 Audio Measurements

- THD and THD+N versus power and frequency.
- Individual harmonic amplitudes, especially H2 through H9.
- CCIF 19/20 kHz and SMPTE 60 Hz/7 kHz IMD.
- A multitone test representative of music.
- 20 Hz to 20 kHz output noise, both unweighted and A-weighted.
- Wideband output noise and switching residual, reported separately from audio-band noise.
- Frequency response, phase response, output impedance, and damping factor versus load.
- Channel separation with the idle channel terminated normally.
- DC offset, startup/shutdown transient, clipping behavior, and clipping recovery.
- Idle spectrum over a long FFT record to reveal oscillator beat products.

Use an appropriate passive Class-D analyzer filter and anti-alias filtering. Always state analyzer bandwidth and weighting so that results remain comparable with EPC's published numbers.

4.4 Switching, Power, EMI, and Thermal Measurements

- High-side and low-side gate-to-source voltage at the FET pads.
- Dead time, reverse-conduction interval, transition time, and any gate overlap.
- Switch-node overshoot, undershoot, ringing frequency, and damping.
- Rail ripple at the PSU, motherboard connector, power-stage connector, local bulk capacitors, and high-frequency commutation capacitors.
- NCP51820 local supply and bootstrap voltage over the full duty-cycle range.
- Input current, idle power, efficiency, and device temperature.
- Near-field E/H scan and common-mode current on input, output, supply, heatsink, and chassis conductors.
- OCP, UVP, OVP, OTP, HF protection, and recovery behavior after every control-loop or gate-drive change.

5. Detailed Recommendations

5.1 External Power Supply and Wiring

1. Follow EPC's recommendation to add approximately 3300 μ F per rail close to the amplifier when the PSU cannot absorb audio-frequency ripple. EPC used 4400 μ F per rail for its audio measurements. Select capacitors for voltage margin, ripple current, ESR, lifetime, and inrush current rather than capacitance alone.

- 2. Feed the two channels from a symmetric star point. Avoid sharing a narrow supply or return conductor between channels.
- 3. Place external bulk capacitors at the board end of long supply leads. A large capacitor at the remote PSU does not remove lead inductance.
- 4. Measure for cable/capacitor resonance. Add intentional damping if needed; do not keep adding parallel low-ESR capacitance blindly.
- 5. Use a quiet, regulated 12 V housekeeping supply. Check whether its differential or common-mode switching products appear at the output.
- 6. Benchmark at reduced power with a low-noise laboratory source to distinguish amplifier noise from PSU noise.
- 7. Keep high-voltage power, speaker output, analog input, and fan wiring physically separated.
- 8. Add controlled pre-charge/inrush limiting if the external capacitor bank is enlarged.
- 9. Monitor both rails during low-frequency high-power testing. Unequal rail pumping can create distortion or trigger protection.

5.2 Input, Shielding, and Gain

- 1. Prefer the balanced XLR input. It rejects ground voltage and cable-coupled switching noise better than RCA.
- 2. Leave the UNBAL GND jumper open for balanced operation. For RCA operation, use the documented 10 ohm/100 nF ground network and verify that it does not create a second chassis-ground path.
- 3. Terminate XLR pin 1/shield to chassis at the connector entry in a future enclosure design. Do not route shield current through the audio reference plane.
- 4. Keep the lower 19.6 dB system-gain setting when the source has enough output level. EPC publishes 40 uV(A) at low gain versus 60 uV(A) at high gain.
- 5. Use a source with equal impedance on the balanced legs. Resistor mismatch converts common-mode RF into differential audio error.
- 6. Keep input cables away from EPC9558P, L1, L2, the switch node, and heatsink.
- 7. Verify the existing 500 kHz motherboard input filter and 100 kHz modulator differential filter with the actual source impedance.
- 8. Do not add large input capacitors without testing RF immunity, audio bandwidth, and op-amp stability.

5.3 D1/D2 Schottky Diodes and R86 Dead Time

This is the most board-specific high-value experiment. EPC states that the parallel Schottky diodes show a reverse-recovery signature above approximately 10 A and that operation without them and with shorter dead time had not yet been evaluated.

The stock setting is R86 = 49.9 kohm, or approximately 50 ns. The NCP51820's internal minimum is approximately 30 ns.

Use this controlled matrix:

Test	Active freewheel diodes	R86 target	Purpose
A	Stock D1/D2	49.9 kohm	Reference
B	Electrically disconnected D1/D2	49.9 kohm	Isolate diode charge effects

Test	Active freewheel diodes	R86 target	Purpose
C	Disconnected D1/D2	About 43 kohm	Reduce reverse-conduction interval
D	Disconnected D1/D2	About 39 kohm	Continue only if C is clean
E	Disconnected D1/D2	About 33 kohm	Near-minimum experiment only after lower-risk tests

Requirements:

- Begin near the minimum recommended rail voltage with a current-limited source and resistive dummy load.
- Confirm actual dead time at both current polarities and over temperature; resistor value alone is not proof.
- Monitor both FET gates, switch node, supply current, overshoot, idle loss, THD, efficiency, and temperature.
- Stop if there is overlap, abnormal current, increased gate disturbance, unsafe overshoot, or erratic protection behavior.
- Repeat at increasing load current because the optimum timing depends on current direction and magnitude.
- Do not operate below the driver's allowed dead time.

D3/D4 are documented as mechanical dummy diodes. The heatsink arrangement uses all four diode packages as height/stability features. Preserve the heatsink standoff, insulation, pressure, and clearance if D1/D2 are removed or electrically isolated. Never allow the heatsink to contact a live node.

5.4 Gate-Drive Optimization

1. Characterize the separate gate paths around $R80/R82 = 3.3 \text{ ohm}$ and $R81/R83 = 0.47 \text{ ohm}$ before changing them. Confirm which path controls turn-on and turn-off from the schematic and waveforms.
2. Tune high-side and low-side values symmetrically unless measured asymmetry justifies otherwise.
3. Evaluate small resistor steps. Faster switching is not automatically better: it can reduce transition loss while increasing ringing, common-mode current, feedback contamination, and FET voltage stress.
4. Probe at the FET gate and source pads with a high-bandwidth differential probe or a very short ground spring. A long probe ground lead creates false ringing.
5. Check gate overshoot, negative gate voltage, Miller-induced turn-on, and driver-ground bounce.
6. Verify the NCP51820 supply and bootstrap rails during clipping and near 100% duty cycle.
7. Do not add ferrite beads to the gates without impedance and waveform measurements. Their nonlinear impedance can create a new resonance.
8. In a PCB revision, minimize each gate loop and provide a Kelvin source return to the driver.

5.5 Power-Stage Decoupling

The existing EPC9558P network is already substantial: Ci1-Ci4 are 10 nF/200 V, Ci5 is 100 nF/250 V, C15/C16 are 1 uF/100 V, and local bulk capacitance is provided by C13a/b and C14a/b.

1. Measure voltage directly across the commutation loop. Connector or remote-rail measurements cannot reveal local bounce accurately.
2. Verify capacitor voltage derating at ± 85 V and temperature, especially the 100 V ceramic parts.
3. Use an impedance analyzer or measured ringing to identify anti-resonances between ceramics, electrolytics, ferrites, and wiring.
4. Add a different package/value only when it fills a measured impedance gap and can be placed in a genuinely smaller current loop.
5. Keep driver bypass current separate from the high-current source path.
6. Measure FB1/FB2 heating and impedance under DC bias. Replace them only if saturation, loss, or modulation is demonstrated.
7. In a PCB revision, place the smallest high-frequency capacitor directly between the FET supply and return nodes with minimum loop area.

5.6 EMI Network and Switch Node

1. Characterize $L1 = 330$ nH at operating current. Its nominal 20 A description is close to the approximately 18.7 A peak current needed for 700 W/4 ohm, while the kit allows larger short peaks. Current-dependent inductance can become an audio distortion mechanism.
2. A/B test L1 only with simultaneous THD, switch-node, and EMI measurements. Bypassing it may reduce magnetic nonlinearity but worsen radiated emissions and ringing.
3. Tune the existing network around L1, R18-R20, C17/C19, and C20/C21 from the measured ringing frequency and damping. Do not select snubber values by trial at full power.
4. Minimize switch-node copper area in a PCB revision while preserving thermal and current capability.
5. Keep feedback, input, enable, clock, and protection traces away from the switch-node copper and the hot end of L1/L2.
6. Do not place a ground shield immediately under the switch node without evaluating the added capacitance and common-mode current.
7. Measure RF voltage on the heatsink. Its capacitance to multiple switching nodes can couple common-mode noise into chassis or nearby wiring.
8. Do not directly earth the heatsink as an experiment unless insulation, fault safety, displacement current, and EMI behavior have been engineered.

5.7 Output Filter and Load Interface

1. Keep the nominal $L2 = 10$ uH and $C18 = 0.68$ uF values for initial experiments. Their ideal resonance is approximately 61 kHz and they are part of the PFFB plant.
2. Measure L2 inductance versus current, minor-loop hysteresis, DCR, core loss, temperature, saturation margin, and harmonic distortion.
3. Compare the approved Codaca and Providence inductors under identical electrical and thermal conditions. Select by measured linearity, not DCR alone.
4. Confirm C18 is polypropylene film and measure capacitance, ESR, and heating. The fitted 450 V part already has ample dielectric quality; a boutique capacitor is unlikely to help.
5. Remember that lower ESR can increase filter Q and reduce phase margin. It is not an unconditional upgrade.
6. Check magnetic coupling between channel inductors. Rotate or separate them in a PCB/mechanical revision if one channel creates measurable output in the idle channel.
7. Use low-resistance speaker connectors and twisted output wiring. Verify contact heating at high current.

8. Confirm that PFFB senses the load side of all meaningful connector/current-sensor resistance. Use Kelvin sensing at the output terminal in a redesign.
9. Evaluate an output Zobel only after measuring load impedance and loop stability. Size it for switching-frequency dissipation and reactive-load behavior.
10. Avoid high-capacitance speaker cables. The official design becomes unstable above 0.2 μF of purely capacitive loading.

5.8 PFFB and EPC9558L Modulator

The inner loop estimates AC inductor current using the output-capacitor voltage network, while the outer voltage loop provides approximately 50 dB DC and 40 dB 20 kHz gain. Small changes can therefore affect switching frequency, loop margin, and protection.

1. Confirm C3 on both boards. Select-match C3 and other critical C0G timing capacitors if channel switching-frequency mismatch is excessive.
2. Measure loop gain and phase margin with 2, 4, and 8 ohm loads, the simulated speaker load, representative cables, minimum/maximum rails, and hot/cold boards.
3. Measure switching spikes on the VOUT feedback signal and at U1/U5 inputs. Look for demodulation or recovery artifacts.
4. Route VOUT and its quiet reference as a tightly coupled Kelvin pair in a PCB revision.
5. Sense at the output terminal after relevant connector and current-sensor resistance if the control architecture permits it.
6. Keep the feedback return separate from gate-drive and speaker-current returns until the intended star/reference point.
7. Consider proportionally reducing high feedback-resistor values and increasing associated capacitors to preserve every pole while lowering Johnson noise. Model op-amp current noise, loading, power, and loop phase before changing values.
8. The existing C0G/NP0 capacitors and thin-film resistors are already appropriate. Preserve dielectric, tolerance, voltage coefficient, and temperature coefficient.
9. Clean flux and contamination around high-impedance feedback nodes; leakage can shift DC gain or create channel mismatch.
10. Do not change C3 merely to raise switching frequency. At high modulation, the switching frequency falls substantially, and all timing, filter, loss, and protection behavior must be revalidated.

5.9 Op-Amps, Comparator, and Logic

1. Do not treat U1/U5 or motherboard U2 replacement as a plug-in audio upgrade. Verify supply range, common-mode range, output current, input noise voltage/current, distortion, GBW, slew rate, capacitive-load stability, overload recovery, and package pinout.
2. ROHM lists LM4565F as last-time-buy, so qualify a production successor even if it does not improve measured audio performance.
3. U3 (LMV7239) propagation delay is part of the self-oscillating loop. A faster or lower-jitter comparator changes switching frequency and phase shift and requires compensation validation.
4. Comparator offset and delay dispersion may contribute to duty-cycle asymmetry. Evaluate alternatives only on an instrumented spare EPC9558L board.
5. Check logic-edge coupling from U2/U4/U6 into analog ground and timing nodes. Series damping should be based on measured ringing.

6. Disabling indicator LEDs during a noise test can determine whether their pulsed currents matter, but retain fault indication in the finished design.

5.10 Analog and Housekeeping Power

1. Measure the +/-12 V op-amp rails and 5 V logic rail with no signal and during high-power output.
2. Search the output spectrum for Mornsun B1212S converter frequency, harmonics, and beat products with the 600 kHz modulator.
3. Add common-mode and differential filtering to the isolated-converter outputs only after checking converter stability and startup.
4. Consider low-noise post-regulation for the analog rails in a PCB revision, with enough headroom and dissipation margin.
5. Keep analog-rail return currents out of the gate-driver and power return paths.
6. Decouple each analog IC locally with the shortest return to its quiet reference plane.
7. Separate logic 5 V filtering from comparator/analog 5 V filtering if measurements show logic-edge contamination.

5.11 Grounding and PCB Layout

1. Treat chassis/shield, audio ground, control ground, driver ground, high-current power return, and speaker return as different current systems.
2. Do not split planes arbitrarily. First map current paths and ground voltage with differential probes.
3. Keep the commutation current local to EPC9558P and the gate-drive return local to NCP51820/FETs.
4. Prevent output and DC-link current from sharing connector pins, vias, or copper necks with PFFB and input returns.
5. Reduce daughterboard connector inductance and contact resistance in a PCB revision, especially for paralleled VDD, VSS, OUT, and ground pins.
6. Preserve an unbroken reference plane under sensitive input, feedback, and PWM routes except where the switch-node field requires a deliberate keepout.
7. Add dense ground stitching around board edges and noisy/sensitive region boundaries only where it supports the intended return path.
8. Validate single-ended and BTL current paths separately. In BTL mode neither speaker terminal is ground.

5.12 Two-Channel Operation and Synchronization

1. Capture both PWM outputs simultaneously over a long record and calculate instantaneous switching frequency and difference frequency.
2. Compare the output spectrum with one and two channels operating. Look for low-frequency beats and intermodulation sidebands.
3. Improve per-channel supply isolation and inductor separation before adding synchronization.
4. The motherboard includes unpopulated clock/synchronization provisions. Do not populate them without confirming the required waveform, frequency range, phase behavior, and EPC9558L injection mechanism.
5. Synchronization can remove beat products but concentrate energy into coherent EMI peaks. Compare conducted/radiated EMI as well as audio measurements.
6. If a redesign permits it, evaluate controlled phase interleaving to reduce shared supply ripple, while verifying PFFB stability and channel timing.

5.13 Thermal and Mechanical Behavior

1. Preserve the specified 0.5 mm high-conductivity TIM, heatsink standoff, approximately 50 psi compression, and electrical isolation.
2. Use the documented 200 LFM airflow for rated 700 W/4 ohm operation. The rating assumes at least 6 dB crest factor and limited burst duration.
3. Map both FETs, driver, D1/D2, L1, L2, ferrites, capacitors, connector pins, and current sensor with calibrated thermal imaging.
4. Compare THD and dead time from cold start to thermal equilibrium.
5. Ensure both channels have similar airflow and heatsink pressure.
6. If a fan is used, power it from a separate filtered supply. Avoid low-frequency PWM fan control that produces audio-band electrical or acoustic modulation.
7. Mechanically secure L2 if vibration is excessive, but do not trap heat or use a magnetic/conductive fastener that changes core behavior.

5.14 Protection and Reliability

1. Keep OCP, OTP, UVP, OVP, integrator-clipping, and HF-instability protection active during development.
2. Verify the installed Hall sensor and actual OCP threshold before full-power tests.
3. Log whether protection reacts to genuine load current or switching spikes after every gate/snubber change.
4. Do not slow OCP or add blanking until short-circuit energy has been calculated and fault-injection tested.
5. Test startup, shutdown, missing rail, unequal rails, clipping, open load, 2 ohm load, reactive load, and output short under controlled conditions.
6. Recheck 200 V FET voltage margin at maximum +/-85 V rails. The nominal switch-node excursion is already 170 V before overshoot.
7. Retain creepage, clearance, insulation, fuse, and touch-safety requirements in any enclosure or PCB revision.

6. Longer-Term Redesign Opportunities

These require new PCB/CAD files and full electrical validation:

1. Reduce the EPC9558P high-frequency commutation-loop area further.
2. Add explicit Kelvin source returns for both FET gate-drive loops.
3. Reduce switch-node copper area and field coupling to the heatsink and feedback network.
4. Route post-filter feedback as a differential/Kelvin pair from the output terminal.
5. Separate each channel's bulk supply path and analog/logic filtering.
6. Replace high-current daughterboard header paths with lower-inductance interconnects or a more integrated board.
7. Optimize L1/L2 orientation and channel spacing for low magnetic crosstalk.
8. Add provision for measurable, selectable dead-time values and diode isolation without compromising heatsink mechanics.
9. Add safe coaxial test points for gate, switch-node, rail, and feedback measurements without introducing long stubs.
10. Model the complete PFFB loop with EPC2307, NCP51820, PCB parasitics, output filter, cable, and representative loudspeaker loads.

- 11. Investigate rail-voltage feed-forward using the existing VDD-SNS/VSS-SNS signals.
- 12. Investigate current-dependent or adaptive dead time only after a fixed-timing optimum is established.
- 13. Evaluate an improved modulator/comparator architecture for lower timing dispersion and idle tones.
- 14. Engineer a defined chassis/heatsink RF connection using safety-rated components if common-mode measurements justify it.

7. Changes Not Recommended Without Evidence

- Blind op-amp rolling.
- Replacing C0G or polypropylene capacitors with physically larger "audiophile" parts.
- Increasing capacitance everywhere without impedance/anti-resonance measurements.
- Raising switching frequency solely because a higher number appears desirable.
- Removing protection circuitry.
- Removing D1/D2 without preserving heatsink mechanics and retuning dead time.
- Removing L1 or snubbers without EMI and FET-stress measurements.
- Cutting ground planes or adding star-ground wires without mapping return currents.
- Directly grounding the heatsink without electrical-safety and common-mode analysis.
- Testing high-power modifications first at +/-85 V.
- Using listening impressions as the only acceptance criterion.

8. Suggested First Experiment Sequence

- 1. Photograph and audit both channels; resolve C3, current sensor, L2, diode, and revision discrepancies.
- 2. Measure the untouched board using the baseline plan.
- 3. Optimize external bulk capacitance, supply wiring, balanced input, grounding, and airflow without modifying the PCB.
- 4. Repeat the baseline to quantify the system-level gain.
- 5. On one spare power-stage board, test D1/D2 connected versus electrically disconnected at stock 50 ns dead time.
- 6. With D1/D2 disconnected, reduce dead time in controlled steps while monitoring both gates and supply current.
- 7. Select the best safe diode/dead-time combination from THD, efficiency, EMI, overshoot, and thermal results together.
- 8. Tune gate turn-on/turn-off impedance around that operating point.
- 9. Characterize L1 and L2 current nonlinearity and compare approved alternatives.
- 10. Measure loop gain before attempting any C3, output-filter, PFFB, comparator, or op-amp change.

9. Experiment Record Template

Field	Value
Test ID/date	
Board/channel/revision	
Modification	
VDD/VSS/12 V supply	
External capacitance/ESR	

Field	Value
Load and cable	
Input mode/gain	
Temperature/airflow	
Switching frequency/dead time	
THD+N/IMD/noise result	
Overshoot/gate result	
Efficiency/temperature result	
EMI result	
Protection result	
Decision	Accept / reject / retest

10. Safety

The board can use +/-85 V rails, produces a 170 V switching excursion before overshoot, and can deliver lethal energy and dangerous sound pressure. Gate-drive, diode, dead-time, and switch-node experiments require qualified high-voltage practice, current-limited startup, insulated tools, non-inductive dummy loads, correctly rated differential probes, safe discharge procedures, eye/hearing protection, and a controlled test area. Do not attach an earth-referenced oscilloscope ground to a switching or BTL output node.

References Reviewed

- [../Official/EPC9192_qsg.pdf](#)
- [../Official/EPC9192_Schematic.pdf](#)
- [../Official/EPC9192BOM.xlsx](#)
- [../Official/EPC9558L_Schematic.pdf](#)
- [../Official/EPC9558LBOM.xlsx](#)
- [../Official/EPC9558P_Schematic.pdf](#)
- [../Official/EPC9558PBOM.xlsx](#)
- Official Gerber, drill, report, stackup, and fabrication files under [../Official/Gerber/](#)
- EPC9192 product page and EPC2307/NCP51820 manufacturer documentation